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10/825,839	04/15/2004	Lee Teck Kheng	MI22-2460	9446

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WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/825,839	KHENG, LEE TECK	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,7,8 and 57-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4,7,8 and 57-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/27/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 2-4, 7, 8 and 57-68 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In lines 12-14 of claim 7, the limitation of "wherein an entirety of the spacing between the uppermost surface of the plurality of the circuit traces and the semiconductor die is completely filed with the adhesive structure," is not supported by or described in the specification. For example, fig. 2 shows a space between the circuit traces 108 and the die 12 which is not filled with adhesive 16. Claims 2-4, 8 and 57-68 depend from claim 7, and thus, are also rejected for the same reasons.

Response to Arguments

2. Applicant's arguments filed on October 27, 2008, are moot in view of new grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-4, 7, 8, 57-61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA), as applied to claim 7 above, in view of Kim (US 2003/0067064).

Regarding claim 7, AAPA discloses a semiconductor package in fig. 1, comprising:

an interposer 14 construction comprising a single dielectric support member 20, a plurality conductive circuit traces 17 contacting the single dielectric support member 20, wherein the entire structure of the single dielectric support member 20 is a single layer of dielectric material (¶ [0004]);

a semiconductor die 12 electrically connected with at least one of the traces 17;

at least one of the circuit traces 17 being between the semiconductor die 12 and the dielectric support member 20;

the single dielectric support member 20 having a first surface and an opposing second surface, fig. 1, the plurality of circuit traces 17 comprising an uppermost surface that is coplanar with the first surface, fig. 1, openings (gaps between support member 20) extending through the second surface to at least some of the circuit traces 17;

contact pads 30 within one or more of the openings and in electrical connection with one or more of the circuit traces 17, the contact pads 30 being entirely contained within the openings, fig. 1, wherein an entirety of at least one of the contact pads 30 is elevationally spaced from at least one of the first and the second surfaces of the of the dielectric support member 20; and solder balls 36 in electrical connection with the contact pads 30; and

wherein the semiconductor die 12 is spaced from the plurality of the circuit traces by an adhesive structure 16, and wherein a part of the spacing between the uppermost surface of the plurality of circuit traces 17 and the semiconductor die 12 is filed with the adhesive structure.

Thus, AAPA discloses all the limitation of the claim with the exception of disclosing wherein an entirety of the spacing between the uppermost surface of the plurality of circuit traces and the semiconductor die is completely filled with the adhesive structure.

However, Kim discloses in fig. 3, a semiconductor package wherein the semiconductor die 210 (¶ [0033]) is spaced from the plurality of the circuit traces 233 (¶ [0036]) by an adhesive structure 227 (¶ [0034]), wherein an entirety of spacing between the uppermost surface of the plurality of the circuit traces 233 and the semiconductor die 210 is completely filled with the adhesive structure 227 (fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the teaching of Kim into the disclosure of AAPA, for the purpose of improving the reliability of the package by preventing the circuit traces

from peeling off, while at the same time reducing the size of the package by directly attaching the circuit traces to the semiconductor die.

Regarding claim 2, AAPA teaches the semiconductor package wherein the support member 20 is a photomask material (specification [0005]: "dry film photomask").

Regarding claims 3 and 64, AAPA discloses all the limitations of the claim with the exception of disclosing: wherein the dielectric support member is not a photomask material, and wherein the dielectric support member comprises at least on of polyimide and liquid polymer crystal. However, Kim discloses a semiconductor package in fig. 3, wherein a dielectric support member 221 comprises polyimide tape (¶ [0034]: "polyimide tape"). Polyimide tape is well known and typically used in semiconductor packages because of their flexibility and adhesive properties.

Regarding claim 4, AAPA discloses all the limitations of the claim with the exception of disclosing: wherein the one or more circuit traces comprise copper. However, Kim discloses a semiconductor package in fig. 3, wherein the circuit traces 233 comprise copper (¶ [0039]: Cu), which is a well known conductive material that provides electrical connections in semiconductor packages.

Regarding claim 8, AAPA discloses the semiconductor package wherein the dielectric support member 20 has a slit 50 extending there through; and the electrical connection of the semiconductor die 12 to said at least one of the circuit traces 17 includes one or more wire bonds 44, extending from the die 12, through the slit 50, and into at least one of the openings (fig. 1).

Regarding claims 57-59, AAPA discloses the semiconductor package wherein the entirety of the at least one contact pad 30 is elevationally spaced from both the first and the second surfaces of the dielectric support member 20 (fig. 1).

Regarding claims 60, 65, and 68, AAPA discloses in fig. 1, wherein the adhesive structure 16 directly contacts the semiconductor die 12 and is comprised of a dielectric material (¶ [0004]). AAPA does not disclose wherein the adhesive structure directly contacts the plurality of the circuit traces and directly contacts the dielectric support member. However, Kim discloses a semiconductor package in fig. 3, wherein the adhesive structure 227 directly contacts the plurality of circuit traces 233, directly contacts the semiconductor die 210, and directly contacts the dielectric support member 221. As stated above, a more stable and reliable package, with reduced size, is obtained by using the adhesive structure, to directly attach the interposer structure to the semiconductor die.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the teachings of Huang into the device of AAPA, because of the advantages set forth above. Furthermore, such modifications are considered well known and conventional in the art of semiconductor devices.

Regarding claim 61, AAPA discloses the semiconductor package wherein the at least one contact pad 30 comprises at least two conductive layers (32 and 34; ¶ [0006]), fig. 1.

Regarding claim 66, AAPA discloses the semiconductor package wherein each solder ball 36 is in physical contact with one contact pad 30 (fig. 1).

Regarding claim 67, AAPA discloses the semiconductor package wherein a portion of each solder ball 36 rests in one of the openings (fig. 1).

4. Claims 62 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Kim (US 2003/0067064), as applied to claim 7 above, and further in view of Yee et al. (US 2003/0230799).

Regarding claims 62 and 63, AAPA and Kim teach all the limitations of the claim with the exception of disclosing wherein the interposer has a thickness comprising a range from about 15 μm to about 150 μm (claim 62) and wherein the interposer has a thickness comprising about 50 μm (claim 63).

However, Yee discloses a semiconductor package (Fig. 1) comprising an interposer 12 with a thickness in range from about 20 μm to about 150 μm (¶ [0047]). Note, where patentability is said to based upon particular chosen range or dimension recited in a claim, the Applicant must show that the chosen range or dimension is critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Furthermore, it is not inventive to discover optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the teaching of Yee into the device of AAPA and Kim, thereby having a thickness of the interposer in such a range as claimed, because

the range is not critical since it can be optimized during routine experimentation, depending upon the desired size of the package.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/A. K./
Examiner, Art Unit 2814

/Phat X. Cao/
Primary Examiner, Art Unit 2814